In the Claims:

1.-3. (Cancelled)

4. (Previously Presented) A device for converting an input signal comprising a bipolar pulse with a positive part and a negative part of same duration into a difference signal, comprising:

a delay member with an input for receiving the input signal and an output, for delaying the input signal to obtain a delayed signal and for outputting the delayed signal at an output;

a differential amplifier with a first input for receiving the input signal, a second input for receiving the delayed signal and an output for outputting the difference signal formed from the input signal and the delayed signal;

wherein the delay member includes a first partial delay member with an input for receiving the input signal and an output for outputting a partially delayed signal and a second partial delay member with an input for receiving the partially delayed signal and an output for outputting the delayed signal;

wherein the differential amplifier further comprises an edge detector for detecting an edge of the partially delayed signal and a comparator for determining whether the difference signal is greater than a first predetermined threshold, for determining whether the difference signal is smaller than a second predetermined threshold; and

wherein the differential amplifier is implemented to output ~~for outputting~~ a binary signal depending on whether the difference signal is greater than the first predetermined threshold and the partially delayed signal comprises a rising edge or whether the partially delayed signal is

smaller than the second predetermined threshold and the partially delayed signal comprises a falling edge.

5. (Previously Presented) The device in accordance with claim 4,

wherein the delay member comprises a plurality of partial delay members, which are connected in series between the input and the output of the delay member, to generate several varyingly strong delayed signals, and

wherein the differential amplifier comprises a plurality of first inputs for receiving a plurality of first input signals and a plurality of second inputs for receiving a plurality of second input signals and wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the first input signal and to select one of the plurality of second input signals to be the second input signal.

6. (Previously Presented) The device in accordance with claim 5, wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the input signal and to select one of the plurality of second input signals to be the second input signal depending on the duration of the positive part and of the negative part of the bipolar pulse of the input signal.

7. (Cancelled)

8. (Original) A device for transmitting a bit, comprising:

a driver for driving the input signal comprising a pulse with a positive part and a negative part of same duration which encodes the bit;

a transmission line for transmitting the input signal with an input, which is connected to the driver, and an output;

a device for converting the input signal into a difference signal, the device comprising a delay member with an input for receiving the input signal and an output, for delaying the input signal to obtain a delayed signal and for outputting the delayed signal at an output, and a differential amplifier with a first input for receiving the input signal, a second input for receiving the delayed signal and an output for outputting the difference signal formed from the input signal and the delayed signal; and

a termination load, which is connected to the output of the delay member.

9. (Original) The device in accordance with claim 8, wherein the termination load is connected to the output of the delay member via a further transmission line.

10.-12. (Cancelled)

13. (Previously Presented) A method for converting an input signal, comprising a bipolar pulse with a positive part and a negative part of same duration, into a difference signal, comprising:

delaying the input signal to obtain a delayed signal;

forming a difference signal from the input signal and the delayed signal;

generating a partially delayed from the input signal, wherein the delay of the partially delayed signal as against the input signal is less than the delay of the delayed signal as against the input signal;

detecting an edge of the partially delayed signal;

determining whether the difference signal is greater than a first predetermined threshold or smaller than a second predetermined threshold; and

outputting a binary signal depending on whether the difference signal is greater than the first predetermined threshold and the partially delayed signal comprises a rising edge or whether the difference signal is smaller than the second predetermined threshold and the partially delayed signal comprises a falling edge.

14. (Previously Presented) The method in accordance with claim 13, further comprising:

generating a plurality of varyingly strong delayed signals; and

selecting of two of the plurality of varyingly strong delayed signals depending on the duration of the positive part and of the negative part of the bipolar pulse to obtain a first selected signal and a second selected signal.

15. (Original) A method for transmitting a bit, comprising:

driving an input signal comprising a pulse with a positive part and a negative part of same duration which encodes the bit;

transmitting the input signal;

converting the input signal into a difference signal, by delaying the input signal to obtain a delayed signal, and forming a difference signal from the input signal and the delayed signal; and

decoding the bit by means of the difference signal.

16. (Previously Presented) A device for converting an input signal comprising a bipolar pulse with a positive part and a negative part of same duration into a difference signal,

comprising:

a plurality of partial delay members, which are connected in series between the input and the output of the delay member, to generate several varyingly strong delayed signals;

a differential amplifier with a first input for receiving the input signal, a second input for receiving the delayed signal and an output for outputting the difference signal formed from the input signal and the delayed signal;

wherein the differential amplifier comprises a plurality of first inputs for receiving a plurality of first input signals and a plurality of second inputs for receiving a plurality of second inputs signals and wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the first input signal and to select one of the plurality of second input signals to be the second input signal; and

wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the input signal and to select one of the plurality of second input signals to be the second input signal depending on the duration of the positive part and of the negative part of the bipolar pulse of the input signal.

17. (Currently Amended) A method for converting an input signal, comprising a bipolar pulse with a positive part and a negative part of same duration, into a difference signal, comprising:

~~generating a plurality of varyingly strong delayed signals;~~

generating a plurality of varyingly strong delayed signals;

selecting of two of the plurality of varyingly strong delayed signals depending on the duration of the positive part and of the negative part of the bipolar pulse to obtain a first selected

signal and a second selected signal; and

forming a difference signal from the input signal and the delayed signal.

18. (Previously Presented) A device for converting an input signal comprising a bipolar pulse with a positive part and a negative part having the same duration into a binary signal, comprising:

delay circuitry comprising a first delay member having an input for receiving the input signal and an output for outputting a partially delayed signal, and a second delay member having an input for receiving the partially delayed signal and an output for outputting a delayed signal; and

differential amplifier circuitry comprising a first input for receiving the input signal, a second input for receiving the partially delayed signal, a third input for receiving the delayed signal, and an output for outputting a difference signal formed from the input signal and the delayed signal, said differential amplifier circuitry further comprising,

edge detector circuitry for determining if said edge of the partially delayed signal is rising or falling, and a comparator circuitry, said edge detector circuitry and comparator circuitry operating to output a binary signal depending on whether the difference signal is greater than a first predetermined threshold and the partially delayed signal comprises a rising edge, or whether the difference signal is smaller than a second predetermined threshold and the partially delayed signal comprises a falling edge.

19. (Previously Presented) The device of claim 18 wherein the delay circuitry comprises a plurality of partial delay members, which are connected in series between the input and the output of the delay member, to generate several varyingly strong delayed signals, and

wherein the differential amplifier comprises a plurality of first inputs for receiving a plurality of first input signals and a plurality of second inputs for receiving a plurality of second input signals and wherein the differential amplifier is implemented to select one of the plurality of first input signals to be the first input signal and to select one of the plurality of second input signals to be the second input signal.

20. (Previously Presented) The device of claim 19 wherein the differential amplifier circuitry is implemented to select one of the plurality of first input signals to be the input signal and to select one of the plurality of second input signals to be the second input signal depending on the duration of the positive part and of the negative part of the bipolar pulse of the input signal.

21. (New) The device of claim 8 further comprising a reference potential, said reference potential connected to said driver and to said termination load and said positive part of said input signal being positive with respect to said reference signal and said negative part of said input signal being negative with respect to said reference signal.

22. (New) The device of claim 21 wherein said reference potential is ground.

23. (New) The method of claim 15 further comprising connecting a reference potential such that said positive part of said input signal is greater than said reference signal and said negative part of said input signal is less than said reference signal.

24. (New) The method of claim 23 wherein said reference potential is ground.